In the Specification:

Please replace the paragraph beginning on page 7 line 23 with the following amended paragraph:

Figures 2 and 5 illustrate the programming of a zero bit in a cell of an EPROM according to a second embodiment of the present invention, in which the storage method parameter is the target threshold voltage. Programming voltage pulse train **12** of Figure 2 is applied to the cell, as in the prior art, but only until the threshold voltage reaches a target value that is sufficiently close to a voltage $\mathbf{V_0'}$ that is less than $\mathbf{V_0}$. Because $\mathbf{V_0'}$ is less than $\mathbf{V_0}$, the cell of Figure 5 is programmed in less time than the cell of Figures 1 and 2, at the expense of the distribution **30** of the resulting floating gate voltages being closer to $\mathbf{V_T}$ than distribution **16**, which is shown in Figure **[[2]]** 5 in phantom for reference. It follows that the lower end **32** of distribution **30** drifts down to $\mathbf{V_T}$ sooner than lower end **18** of distribution **16**; but if it takes much longer than *e.g.* one month for lower end **32** to drift down to $\mathbf{V_T}$, this embodiment of the present invention is suitable for storing data, such as "cached" Web pages, that need to be archived for only one month. Data that need to be archived for many years are programmed as illustrated in Figure 1.